Relationship between trapping density and open circuit voltage in multicrystalline silicon solar cells

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Minority carrier trapping frequently exists in solar grade multicrystalline silicon. At low illumination levels, the effect of trapping centers on open circuit voltage of multicrystalline silicon solar cells is dependent on the trap density and illumination level. In this paper, the relation between trapping density and open circuit voltage of multicrystalline silicon solar cells at different illumination levels is studied by a series of experiments. The experimental evidence suggests that the effect of trapping on open circuit voltage of multicrystalline silicon solar cells is obvious at carrier injection levels equal to and below the trap density, the trapping effect of multicrystalline silicon can be reflected by measuring open circuit voltage at low illumination levels, instead of complicated lifetime measurements, and some multicrystalline silicon solar cells with higher trap densities have higher open-circuit voltages at weak illumination levels. The measurement and analysis of the trapping effect is a relative tool to diagnose the quality of multicrystalline silicon, so a new method is presented to analyze relative quality of multicrystalline silicon by measuring open circuit voltage at weak illumination levels.

1. Introduction

During the 1950s, Haynes and Hornbeck developed a simple trapping model that explained the effect of trapping on drift mobility measurements, and also on steady state and transient photoconductance decay lifetime measurements, which often observed in single crystalline silicon due to the relatively poor quality of the material [1]. According to their model, minority carrier trapping centers mean the states in the energy gap which temporarily hold minority carriers, but do not serve as recombination center. Modern float-zone silicon is no longer plagued by trapping effects, but solar grade multicrystalline silicon very often is, owing to the presence of grain boundaries, point defects, transition metal impurities, oxygen, carbon, and their complexes [2–4]. The trapping centers of multicrystalline silicon often cause a drastic increase in photoconductance at carrier injection levels equal to and below the trap density, and result in a higher open circuit voltage of multicrystalline silicon solar cells than would be the case when traps are absent at low illumination levels below about 0.2 suns [2]. In this paper, the relation between trapping density and open circuit voltage of the mid and low quality multicrystalline silicon at different illumination levels is studied systematically, the experimental evidence suggests that the effect of trapping on open circuit voltage of multicrystalline silicon solar cells is obvious at carrier injection levels equal to and below the trap density, the trapping effect of multicrystalline silicon can be reflected by measuring open circuit voltage at low illumination levels, instead of complicated lifetime measurements.

In this study, the relation between open circuit voltage and the density of trapping centers is investigated at low injection levels after plasma etching away of edge parasitic junctions. Minority carrier trapping centers that are boron-related can be removed by phosphorus gettering, the open circuit voltage at low illumination levels were measured before and after phosphorus gettering, so as

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to reveal its effect on trap density. In the meantime, the effects of cross-contamination experiments and SiNx:H passivation on trap density are also examined by measuring open circuit voltage at low illumination levels. The experiments prove that some multicrystalline silicon solar cells which have higher trap density have higher open circuit voltage at weak illumination levels, this is in agreement with [5].

2. Theoretical background and discussion

Before entering the details of the experimental technique, some discussion is needed about the theoretical relationship between trapping density and open circuit voltage in multicrystalline silicon solar cells.

From a theoretical standpoint, for p-type multicrystalline silicon, as the carrier concentration decreases to near and below the trap density N_t, the proportion of electrons in the traps rises, charge neutrality requires that $\Delta p = \Delta n + n_t$, where n_t is the trapped electron concentration, i.e. trapping centers result in a certain proportion of minority carriers being removed from the recombination channels, resulting in an increase in the concentration of majority carrier, in turn causing a large photoconductance [4]. Hence, as the trapped electron concentration begins to be appreciable, the excess hole concentration becomes significantly higher than the level that would be expected without traps. The result is a larger photoconductance, the excess conductivity $\Delta\sigma$ is

$$\Delta\sigma = q\Delta n(\mu_n + \mu_p) + qn_t\mu_p \tag{1}$$

Where μ_n and μ_p are the electron and hole mobilities, q is the electron charge [5].

The open circuit voltage V_{oc} is

$$\begin{aligned} V_{oc} &= \frac{1}{q}\left[E_{Fn}(x_n) - E_{Fp}(x_p)\right] \\ &= \frac{kT}{q}\left[\ln(n_p/n_i) + \ln(p_p/n_i)\right] \\ &= \frac{kT}{q}\ln\left(n_p p_p/n_i^2\right), \end{aligned} \tag{2}$$

where x_n and x_p are the locations of the n- and p-type contacts, k is Boltzmann's constant, and T is the temperature in degrees Kelvin, n_i is the intrinsic carrier density, $n_p \cong \Delta n$, $p_p = N_A + \Delta n + n_t$, so V_{oc} as an approximation becomes

$$V_{oc} \cong \frac{kT}{q}\ln\left[\frac{\Delta n(N_A + \Delta n + n_t)}{n_i^2}\right] \tag{3}$$

It is interesting to note that, in principle, carrier trapping could be beneficial to device voltage, a simple way to interpret the effect of tapping is, according to Eq. (3), to consider that it is equivalent to an increased dopant density $N_A + n_t$ [3]. With the increasing of illumination levels ($\Delta n > n_t$), the effect of trapping on open circuit voltage is ignored, we would not expect the presence of traps to noticeably affect open circuit voltage, particularly at illumination levels above 0.2 suns, but the effect of traps on open circuit voltage is obvious at low illumination levels.

For the multicrystalline silicon wafers with about $1\Omega\cdot\text{cm} - 5\Omega\cdot\text{cm}$ resisitivity, the dopant concentration of grain is about 10^{15} cm^{-3}, the multicrystalline silicon solar cells would be operating at carrier densities well below 1×10^{15} cm^{-3}, i.e. lower carriers injection. If the range of trap density is from 10^{14}cm^{-3} to 10^{16} cm^{-3}, considering the case of p-type silicon grain at 300 K with $n_i \cong 1.45\times10^{15}$ cm^{-3}, then the effect of trap density on open circuit voltage is no longer unnoticeable at low illumination levels.

At low illumination levels below about 0.1 suns, for $\Delta n << N_A$, so Eq. (3) reduces to

$$V_{oc} \cong 26\ln\left[\frac{\Delta n(10^{15} + n_t)}{2.1\times10^{20}}\right] mV \tag{4}$$

Eq. (4) proves that the trap density can be reflected by open circuit voltage at low illumination levels, particularly when $n_t > 10^{15}$cm^{-3}.

3. Experimental methods

The multicrystalline silicon wafers used in these experiments were grown by directional solidification, the wafers have an area of 100×100 mm^2 with about 1.5Ω·cm resisitivity, and typically have grain sizes ranging from one millimeter to three centimeters, and have different contamination levels, crystallographic qualities. The wafers come from standard solar grade ingots that are typical of those processed commercially into cells, and were labeled by number. Due to the columnar growth of the grain, the distribution of impurities and the density of defects are very similar in these wafers.

The quasi-steady-state photoconductance technique (QSSPC) is well suited for taking 'averaged' measurements on highly inhomogeneous material like multicrystalline silicon [5–6], apparent minority carrier lifetime increases rapidly due to the relative build-up of majority carriers caused by the minority carrier traps, such dramatic injection level dependence is diagnostic of trapping effects [2]. In our experiments, the minority carrier trap density was measured using the QSSPC.

First, the multicrystalline silicon wafers were etched in a CP4 acid solution in order to remove the saw damage, followed by a standard RCA cleaning, the surface of the wafers were then passivated with a thin dry oxide for measuring the trap density, in this process, about 1 % water steam was added to enhance quality of oxide [7].

After the initial trap density measurements, the passivating layers were etched off, and phosphorus diffusion

was performed in an open tube furnace using a $POCl_3$ liquid source, diffusion resulted in an 50-55Ω/□, then edge parasitic junction was etched by plasma of CF_4. Open circuit voltages of these cells were measured at low illumination levels after plasma etching of edge parasitic junction.

The phosphorus glass layers of other cells were then etched off using HF solution after measurements of open circuit voltage at low illumination levels, Gettering was performed by a heavy phosphorus diffusion at 900°C for 3 hours, the gettering layers were subsequently etched off and the wafers were re-passivated with another oxide layer as above. The trap densities of the wafers were then measured again.

Finally, after the passivating layers were etched off, the phosphorus diffusion and the etching of edge parasitic junction were performed again, the open circuit voltages of these cells were re-measured at low illumination levels again, identical to the above.

Cross-contamination experiments were performed by using float-zone wafers of 1Ω·cm resistivity, these float-zone wafers were divided into two groups (1 and 2), the wafers of group 1 were given a cross contamination experiment, each multicrystalline silicon wafer was 'sandwiched' between two float-zone wafers, which absorb out-diffusing impurities from adjacent multicrystalline silicon wafer, and then these wafers were given a light phosphorus diffusion at 900°C for 30 min followed by thin oxide layer growth at 900°C for 30 min [6]; the wafers of group 2 were given a light phosphorus diffusion at 900°C for 30 min followed by thin oxide layer growth at 900°C for 30 min. At last, the etching of edge parasitic junction for float-zone wafers of two groups were performed, open circuit voltage of these cells were measured at low illumination levels.

SiNx:H thin films were prepared by plasma enhanced chemical vapour deposition(PECVD) using SiH_4, NH_3 and N_2. The annealing of the SiNx:H was performed through a rapid thermal processing(RTP) at about 760°C for a short time. The imaginary part (extinction coefficient) of these films is nearly zero in the measured wavelength region of 0.3 to 0.8 um, the refractive index is 2.0 at a wavelength of 632.8 nm.

4. Results and discussion

4.1. Relation between trap density and open circuit voltage of multicrystalline silicon solar cells

Fig. 1 illustrates the open circuit voltages versus trap density for the sample at different illumination level. As the illumination increases, the open circuit voltage of the sample increases.

From Fig. 1, we found that the open circuit voltage rises with the increasing of trap density at the same illumination level, so we could predict the trap density by measuring the open circuit voltage at a certain low illumination level before PECVD SiNx:H relatively.

Fig. 1 also shows that, as the illumination increases, the open circuit voltage of the sample increases.

And for the sample in Fig. 1, when the illumination level is larger than 0.2 suns illumination, the open circuit voltage of the samples eventually approaches the open circuit voltage under standard test conditions of 1000W/m^2, 25°C cell temperature and 1.5 air mass.

The above results agrees approximately with Eq. (4).

4.2. Effect of gettering on open circuit voltage at low illumination levels

Minority carrier trapping centers of boron-related can be removed by phosphorus gettering[5], according to

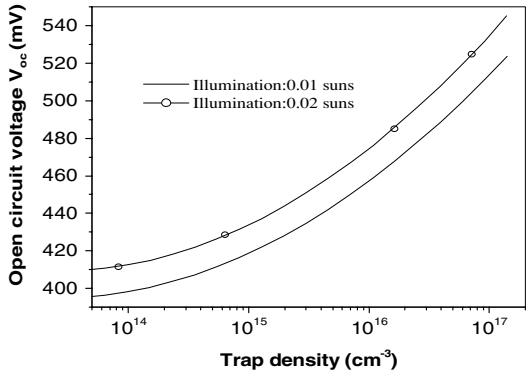

Figure 1 Open circuit voltage versus minority carrier trap density.

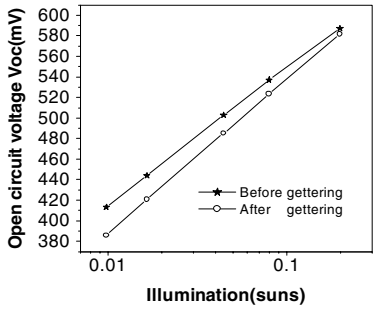

Figure 2 Open circuit voltage of the same multicrystalline silicon wafer versus illumination before and after phosphorus gettering.

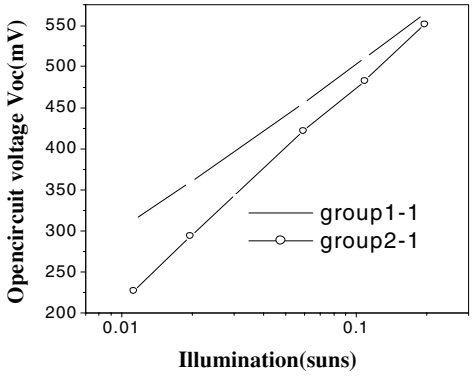

Figure 3 Open circuit voltage of group1-1 and group 2-1 versus illumination.

TABLE I Comparison of open circuit voltage for two groups samples at 0.01 illumination level

Samples	Voc(mV)					
group 1	369	363	364	368	365	364
group 2	341	349	347	345	343	340

TABLE II Comparison of open circuit voltage at 0.01 suns illumination level before and after SiNx:H passivation

Samples	Voc(mV)					
Cells before passivation	407	404	405	408	403	404
Cells after passivation	391	383	389	388	383	385

above results, this phenomenon was reflected by measuring open circuit voltage. Fig. 2 gives the open circuit voltage measured at low illumination levels for the same multicrystalline silicon wafer before and after phosphorus gettering.

For the sample in Fig. 2, note that the open circuit voltage of this sample after gettering is smaller than that before gettering at the same illumination level below about 0.02 suns. This is most likely due to that the gettering treatment reduces the trap density in multicrystalline silicon wafer. The study of open circuit voltage at low illumination levels may become a simple tool to diagnose the trapping density, instead of complicated lifetime measurements.

Boron-related minority carrier trapping centers can be removed by phosphorus gettering, this phenomenon can be reflected by measuring open circuit voltage at weak illumination levels.

4.3. Cross-contamination experiments

Fig. 3 shows open circuit voltage of group 1-1 and group 2-1 versus illumination, Table I gives the comparison of open circuit voltage for two groups samples at 0.01 illumination level. Note that open circuit voltage of group 1 at low illumination levels is higher than that of group 2, the important result is that trap centers are evident in these cross-contaminated float-zone wafers, the open circuit voltage of p-type single crystal float-zone wafers of the cross-contamination experiments at low illumination levels are a clear indication that trap-causing impurities have effused into the float-zone wafers from the multicrystalline silicon wafers, the measurements of voltage is easily performed, instead of the complicated measurement of lifetimes. This experimental result is in agreement with [8].

4.4. Effect of SiNx:H passivation on open circuit voltage at low illumination levels

Table II gives a comparison of open circuit voltage for six samples at 0.01 suns illumination level before and after SiNx:H passivation.

From Table II, we found that open circuit voltage of samples become small after PECVD SiNx:H passivation. This is because SiNx:H contains 10 to 30 % atomic hydrogen, these atomic hydrogen can passivate dangling bonds associated with the defects, and probably reduce dislocation-related trap density [4].

5. Conclusions

Multicrystalline silicon is a complex semiconductor system, the origin of minority carrier traps of multicrystalline silicon is still uncertain, with preliminary evidence indicating that they are related to the crystallographic quality of the material, including grain size, dislocation density and micro-defects, and also to metal impurities. The effect of trap density on open circuit voltage of multicrystalline silicon solar cells is obvious at low illumination levels, then the poor quality wafers may be found by measuring open circuit voltage at low illumination levels before PECVD SiNx:H deposition, instead of complicated lifetime measurements. Boron-related minority carrier trapping centers in solar grade multicrystalline silicon can be removed by phosphorus gettering, this is simply proved by measuring open circuit voltage at low illumination levels, instead of complicated lifetime measurements. The result of cross-contamination experiments can also be proved by measuring open circuit voltage at low illumination levels. These experiments also aid in the evaluation of some special treatments such as phosphorus gettering and hydrogen radical annealing before screenprinting and firing.

In actual production, in-line monitoring of the fabrication process of crystal silicon solar cells is very difficult, at present, there is no adequate and simple method of in-line measurement in the process of fabricating crystal silicon solar cell. The trap density can be represented by measuring open circuit voltage at a low illumination level, The study of open circuit voltage at low illumination levels may become another simple tool to diagnose the quality of multicrystalline silicon in-line for cell producers, instead of complicated lifetime measurements. This method presented by us is also relative, and it is only valuable for the same batch wafers processed by the same process.

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